REMARKS

Reconsideration and allowance of the above-referenced application are respectfully requested.

Applicants thank the Examiner for the telephonic interview that held on July 23, 2002. As requested, comments below are made that explain the patentably distinct aspects of the present invention.

Claim 2 stands rejected under 35 USC 112, second paragraph, as being indefinite. Applicants have amended claim 2 and, as amended, submit that this claim is definite and readily understandable. As written, claim 2 now recites "[T]he system of claim 1, wherein the software development tools generate code to run on the processor." In other words, the "means for, based on the configuration specification, generating software development tools specific to the hardware implementation" as recited in claim 1 will further develop software development tools that generate code to run on the processor. An example of the software development tools that fall within the scope of claim 2 would be a compiler, linker and an assembler. Withdrawal of this rejection is respectfully requested.

Claims 1-21, 23-64, and 66-104 stand rejected under 35 USC 102(b) as being anticipated by Hartoog. Claims 22 and 65 stand rejected under 35 USC 103(a) as being unpatentable over Hartoog. Applicants respectfully traverse the Examiner's rejection.

Applicant's previous amendment response clearly asserted that Hartoog does not generate a description of a hardware implementation of a processor as recited in claim 1. These comments were also applicable to claim 104.

The Examiner continues to reject claims 1 and 104 . As was discussed during the interview, from a single configuration specification (discussion on this provided below), the present invention obtains two different outputs that are related to the processor that is generated. One of these outputs is the recited "hardware implementation" of the processor. The other is the recited "software development tools specific to the hardware implementation." Applicants stressed that while there are systems that provide for the hardware implementation of a processor, and while there are other systems that provide for software development tools, that Hartoog does not teach or suggest a system or method that obtains both of these from a configuration specification as recited.

In the rejection at paragraph 5, it appears that the Examiner asserts that the "configurable specification" is the "(single description of a processor in [the] abstract" of Hartoog. Initially, the invention does not claim a "configurable specification," but a "configuration specification." And the present invention generates a processor, which is a different thing from designing a processor. The design of a broad class of processors is done by hand in the traditional way. The present invention, however, is used to generate a member of this class by applying the parameters from the configuration specification, and then extending the result as recited.

As was discussed during the interview, and as described in the specification at, for example, page 30, lines 5-7, the configuration specification includes parameters set and extensible features that are desired. A description of various configuration options are discussed throughout the specification. Accordingly, this term is clearly defined by the specification and is definite and understandable.

The "single description" in Hartoog is not properly characterized as the configuration specification. "Single description" in the context of Hartoog is directed to the "consistent set of retargetable development tools" that Hartoog would like to see available "for a variety of processors," as discussed in the first paragraph of the "Introduction" at page 303. As was discussed during the interview, the Hartoog "retargetable development tools" operate on already existing processors (the TMS320C50 and ARM 7 are mentioned in the abstract). Thus, this "Single description" is not used to generate hardware. And it is also clear that the "development tools" of Hartoog are not directed to tools for generating hardware, but tools used with respect to instruction sets, such as an instruction set simulator, disassemble, and assembler. And many of these tools were never even built, such as the "Code Generator" and a "Code Retargeter." It is also very clear that the Hartoog reference does not teach how to make these tools.

Continuing with the Examiner's comments at paragraph 5, it is asserted that "nML is a high-level language at abstraction level the processor architecture, where the processor is a hardware.) Respectfully, Applicants do not understand what the Examiner means by this phrase. Accordingly, Applicants have referred to the Examiner's comments at paragraph 22 for further explanation. In those comments, the Examiner asserts that "[Examiner respectfully submits that the nML language can be translated into hardware description language such as VHDL or Verilog, wherein the VHDL or Verilog is supported by well known logic synthesis. Respectfully, nothing in Hartoog teaches or suggests that. It appears that this conclusion has been reached as a result of

the premise that the Examiner started from, the premise being that "[T]he nML is a high-level description language to describe the processor." To the extent that nML is an instruction set description language, the previous sentence of the Examiner would be correct. But to the extent that this is used as a basis to imply that nML can be used to generate a hardware implementation of a processor, based on a configuration specification, it is not.

Applicants desired to confirm that their belief's regarding nML as discussed above were correct to accurately respond to the Examiner's arguments. As such, applicants obtained articles [3] and [4] referenced in Hartoog and these articles are attached in an accompanying Information Disclosure Statement. The "abstract" of article [4] states:

> "nML is a formalism targetted for describing arbitrary single-processor computer architectures. nML works at the instruction set level, i.e. it hides implementation issues of the actual machine...." (Emphasis added)

And in the article [3], it states, for example:

> VHDL is a standardized language with considerable semantic richness. ...All of the above-mentioned hardware description languages require a detailed knowledge of the processor netlist and the instruction decoder. However, this information is usually not available, nor is it necessary for the tasks of code generation and instruction set simulation. (Emphasis added)

These articles clearly support Applicant's position that Hartoog is not directed to generating a description of a hardware implementation of the processor based on a configuration specification and generating software development tools specific to the hardware implementation as recited in claims 1 and 104.

In the Examiner's comments at paragraph 22 the Examiner also asserts that in order to design a processor it takes more than two means as recited in the claims. It is unclear to Applicants whether this is a further rejection of claim 1 and claims dependent thereon, but applicants position is that the system claimed in claim 1 (and the method claimed in claim 104) contains a combination that is novel and non-obvious. In any event, however, and as discussed above, the present invention generates a processor, which is a different thing from designing a processor. Accordingly, applicants submit that the claim is appropriate.

The Examiner also states in paragraph 22 that "[T]he claimed invention is so broad." Again, it is unclear to Applicants whether this is a further rejection of independent claims 1 and 104 and the claims dependent thereon. That said, these claims are an aspect of the core business of the assignee, Tensilica, Inc. And this is not an insignificant business. Tensilica, Inc. has been named to the Red-Herring's list of 100 companies in each of 2000 and 2001. This success is based in part on the implementation of the inventions recited herein.

Applicants further note the Examiner's invitation to the Applicants to define specific means and define the specific configuration specification as set recited in the claims. Applicants respectfully decline the Examiner's invitation. The claims as recited are definite and readily understandable to one of ordinary skill in the art, and further limiting them is not believed necessary.

The rejections of the dependent claims also further confirm the applicants' position.

In rejecting claims 2-13, the subject matter of the claims is repeated in the rejection, and then reference is made to pages 303-305 of Hartoog. As pages 303-305 are almost the entire Hartoog article, this provides no specificity as to where in Hartoog there is a teaching of the subject matter of these claims.

In rejecting claims 14-20 in paragraph 7 of the Office Action, the Examiner initially states that "Hartoog et al teaches implementing hardware design from high level description language." As noted above, this is not accurate, and, as such, this rejection is therefore not appropriate.

The same incorrect premise is used in rejecting claim 21. While the Examiner asserts that ""Hartoog...inherently includ[es] means for synthesizing logic and means for placing and routing, Applicant again respectfully submits that this rejection illustrates a fundamental difference between Hartoog and the present invention is not appreciated: Hartoog's tools are intended to operate on an existing processor and do not teach or suggest generating a description of a hardware implementation of the processor based on a configuration specification and generating software development tools specific to the hardware implementation.

And with respect to claim 22 (rejected on obviousness grounds) that is dependent on claim 21, the tools of Hartoog are not directed to verifying timing of the circuit and determining the area, cycle time and power dissipation of the circuit, as the tools of Hartoog are not directed to implementing hardware, as has been discussed above.

In rejecting claims 23-32, the Examiner asserts that Hartoog teaches generating the configuration specification, as Hartoog etal teach "it could be reconfigured for bit width, number of registers, number of ALU's etc. It appears that the Examiner is reciting certain language from the claims, and then simply reciting what Hartoog can do without regard to the context in which Hartoog is operating and without an appreciation of the fundamental differences between Hartoog's context as noted above and that of the applicants invention. In particular, the Examiner's reference to the "DSP processor on page 303 illustrates this point, since the "DSP processor on page 303" is an existing processor that the tools of Hartoog can operate upon, which reinforces applicants position above that Hartoog does not teach or suggest generating a description of a hardware implementation of the processor based on a configuration specification and generating software development tools specific to the hardware implementation.

And with respect to specific claims, claim 23 further comprises means for generating the configuration specification, and claims 24 and 25 further define the generation of the configuration specification, with claim 24 requiring that the means for generating the configuration specification is responsive to selection of configuration parameters by a user, and claim 25 requiring that the means for generating the configuration specification is for generating the specification based on design goals for the processor. That such a configuration cannot exist is further evident from the fact that separate nML descriptions are needed for each different processor. Accordingly, while two different nML descriptions may be very similar, they must be distinct, in contrast to the configuration specification as recited that can be used to design different processors. From this, it is apparent that the parameter specification in claims 26 is entirely different than any teaching in Hartoog.

The same context differences exists with respect to the Examiner's rejection of claims 33-43, 44-46, 47-54, and 55-59. And each of these claims are ultimately dependent on claim 26. discussed above.

Claims 60-64 and 66-68 further recite means for evaluating suitability of the configuration specification, and aspects related thereto. While the Examiner again repeats the subject matter of these claims in the rejection and simply refers to pages 303-306, these concepts are nowhere taught or suggested by Hartoog.

With respect to claims 69-71, as Hartoog does not contain means for, based on a configuration specification, generating a description of a hardware implementation of the processor, it does not teach or suggest the further aspects of these claims.

Claims 72-91 are directed to the generation of a configuration of the processor by extension (claim 72) and having a configuration specification that includes an extension specification of an extensible characteristic of the processor (Claim 73). Claims 74-91 are ultimately dependent on claim 73. The Examiner's statement regarding Hartoog "generating a good suite of development software tools from processor descriptions for a variety of processors for hardware/software codesign through a retargetable approach ...." is based on the same incorrect premise relating to Hartoog as discussed above. While the tools of Hartoog may be able to be "reconfigured for bit width, number of registers, number of ALU's etc." as noted by the Examiner, this is in the context of applying these tools to different existing processors that may each have different bit width, number of registers, number of ALU's etc. Accordingly, these claims are distinct from any teachings in Hartoog as well.

With respect to claims 92-100, these claims refer to a portion of the configuration specification that is specified by an instruction set architecture description language description Hartoog does not discuss generating a description of a hardware implementation of the processor based on a configuration specification as has been discussed, and thus has an entirely distinct usage from that set forth in claim 92. As such, the same comments made with respect to claims 72-91 also apply to the Examiner's rejection of claims 92-100.

Claims 101-104 combine together the configuration specification that includes a parameter specification specifying a modifiable characteristic and at least extension specification. Each of the parameter specification and extension specification have been discussed above individually as being distinct from Hartoog, and their combination is also distinct, for the same reasons provided.

In view of the above amendments and remarks, applicants submit that the above-referenced application is in a condition for allowance, and such a Notice is respectfully requested.

CHARGE STATEMENT: The Commissioner is hereby authorized to charge fees that may be required relative to this application, or credit any overpayment, to our Account 03-3975/Order No. 083818/0239357).

Respectfully submitted,

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APPENDIX

VERSION WITH MARKINGS SHOWING CHANGES MADE

2. (Twice Amended) The system of claim 1, wherein the software development tools [are for generating software development tools to] generate code to run on the processor.